```
RCS file: /s6/cvsroot/euterpe/BOM,v
Working file: BOM
head: 5.105
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 1940;  selected revisions: 14
description:
top level BOM
----------------------------
revision 3.849
date: 1995/06/15 16:45:57;  author: jeffm;  state: Exp;  lines: +2 -2
Release Target: euterpe/verify/nasty

Oops, prior release contained downlevel files.
----------------------------
revision 3.848
date: 1995/06/15 16:42:58;  author: jeffm;  state: Exp;  lines: +2 -2
Release Target: euterpe/verify/nasty

Fixed hermnasty.
----------------------------
revision 3.847
date: 1995/06/15 00:12:04;  author: bobm;  state: Exp;  lines: +2 -2
Release Target: euterpe/doc
      front.mif
      intro.mif
      opcodes.mif
      pipeline.mif
      memory.mif
      events.mif
      reset.mif
      clock.mif
      cerberus.mif
      endian.mif
      newchanges.mif

only a few small changes
----------------------------
revision 3.846
date: 1995/06/14 22:36:03;  author: mws;  state: Exp;  lines: +2 -2
Release Target: euterpe/verilog/bsrc

uu/uu_control.pim:
  Update for 15jun95's uu/uu.V uu/uuthruut.Veqn uu/uustepuu.pla:
  Change in bsrc BOM 320.1-320.2/321.0 and bsrc/uu BOM 206-7.0 to try to
  suppress forward progress before new store&swap algorithms set its repel
  state still was not working.  It was needed on eta3 but the addition
  of a pipeline that could support eta3 was forgotten and eta0 pipe was
  improperly sustituted.  Change swpBsy pipe to flops to handle all etas.
  Then ustepuu loses 1 dontcare step, but uuthruut can dontcare eta3 enforcement
  on step 1 (restore 1.12).  Hopefully this will stop synch ops from losing CC
  in the middle of their algorithms, (cachesynchnasty_0 performance 50% worse).
cj/rupt.tst cj/rsrvd.tst:  Delay expected event mode exit from BBack
  to BBackBrk to match bsrc/BOM 319.0 and uu/BOM 204.0.
```

```
----------------------------
revision 3.845
date: 1995/06/14 08:39:54;  author: mws;  state: Exp;  lines: +2 -2
Release Target: euterpe/verilog/bsrc/uu

uu/uu.V uu/uuthruut.Veqn uu/uustepuu.pla uu/sswap(8).tst:
  Change in bsrc BOM 320.1-320.2/321.0 and bsrc/uu BOM 206-7.0 to try to
  suppress forward progress before new store&swap algorithms set its repel
  state still was not working.  It was needed on eta3 but the addition
  of a pipeline that could support eta3 was forgotten and eta0 pipe was
  improperly sustituted.  Change swpBsy pipe to flops to handle all etas.
  Then ustepuu loses 1 dontcare step, but uuthruut can dontcare eta3 enforcement
  on step 1 (restore 1.12).  Restore sswap(8).tst to match (125.4(169.2))
  only to avoid confusion of BOM not using newest files).
  Do placement tomorrow.  Hopefully this will stop synch ops from losing CC in
  the middle of their algorithms, (cachesynchnasty_0 performance 50% worse).
----------------------------
revision 3.844
date: 1995/06/13 19:56:53;  author: jeffm;  state: Exp;  lines: +2 -2
Release Target: euterpe/verify/toplevel
      uunb_debug.srl

For debugging uu/nb handshake
----------------------------
revision 3.843
date: 1995/06/13 18:27:42;  author: jeffm;  state: Exp;  lines: +2 -2
Release Target: euterpe/verify/toplevel
      hermnasty_debug.srl

Fix more signal names
----------------------------
revision 3.842
date: 1995/06/13 18:24:45;  author: jeffm;  state: Exp;  lines: +2 -2
Release Target: euterpe/verify/toplevel
      ife_debug.srl

For hermestestC0M0
----------------------------
revision 3.841
date: 1995/06/13 18:07:52;  author: jeffm;  state: Exp;  lines: +2 -2
Release Target: euterpe/verify/toplevel
      hermnasty_debug.srl

Fix signal names
----------------------------
revision 3.840
date: 1995/06/13 17:49:48;  author: jeffm;  state: Exp;  lines: +2 -2
Release Target: euterpe/verify/toplevel
      hermnasty_debug.srl

New trace file for Zycad
----------------------------
revision 3.839
date: 1995/06/12 04:52:26;  author: mws;  state: Exp;  lines: +2 -2
Release Target: euterpe/verilog/bsrc

uu/uu_control.pim for uu/uu.V uu/uuthruut.Veqn uu/uustepuu.pla(comments only)
```

```
----------------------------
revision 3.838
date: 1995/06/11 19:36:29;  author: mws;  state: Exp;  lines: +2 -2
Release Target: euterpe/verilog/bsrc/uu

uu/uu.V (do placement later):
  Change in bsrc BOM 320.1 and bsrc/uu BOM 206.0 to "use the swpBsy pipe to
  suppress forward progress early in the store&swap until the repel can take
  over" was allowing a store&swap (synch op) in one cyl to suppress forward
  progress in up to 3 other cyls.  The claim was that this would not matter
  architecturally, although it would perturb micro level behavior.  Further
  reflection has deemed this too tricky, so add eta chopper so that only the
  cyl needing suppression gets it.
uu/sswap.tst uu/uusswap8.tst:  Restore previous versions to match restore of
  1st job in store&swap again enforcing eta3.  Doing restore only to avoid
  confusion of the BOM including not-the-newest file from the repository.
----------------------------
revision 3.837
date: 1995/06/11 08:36:35;  author: mws;  state: Exp;  lines: +2 -2
Release Target: euterpe/verilog/bsrc/uu

uu/uu.V uu/uuthruut.Veqn uu/uustepuu.pla(comments only)  (do placement later):
  Change in bsrc BOM 319.0 and bsrc/uu BOM 204.0 to "set repel and enforce eta
  for the remaining volatile synch op (store&swap) sequence at the end of the
  2nd (was 1st) job" inadvertently allowed forward progress to be declared,
  releasing CC after an ICache miss before DCache miss was tested.  This
  allowed another cyl to steal the ICache line, undoing the previous fill
  and causing a thrash hang.  To avoid the expense of adding a forward
  progress pipe, we justify the use of the swpBsy pipe to suppress
  forward progress early in the store&swap until the repel can take over.
----------------------------
revision 3.836
date: 1995/06/10 09:08:24;  author: mws;  state: Exp;  lines: +2 -2
Release Target: euterpe/verilog/bsrc

StoreSwaps (atomic/synch ops) were mostly broken because:
uu/uu.V:
  Pipelining typo in yesterday's change used stepUV instead of UW in computing
  vldSwpGoUW, causing probable excess repel toggels leaving preempts locked
  out (hangs) or sequences unprotected (integrity damage).
uu/uustepuu.pla:
  Yesterday's change forgot to remove dontcares no longer available when
  storeswap repel begin delay was overloaded onto swpBsy.
uu/uuswap.tst uu/uuswap8.tst:  Update to match yesterday's change to wait until
  step=1 to align eta and begin repel.
=============================================================================

RCS file: /s6/cvsroot/euterpe/compass/layouts/lid_euterpe_1.ly,v
Working file: compass/layouts/lid_euterpe_1.ly
head: 2.14
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 14;    selected revisions: 1
description:
----------------------------
```

```
revision 2.4
date: 1995/06/14 16:35:41;  author: chip;  state: Exp;  lines: +1920 -58208
periodic checkin of Wed Jun 14 09:35:27 PDT 1995
=============================================================================

RCS file: /s6/cvsroot/euterpe/compass/layouts/vlsi.cko,v
Working file: compass/layouts/vlsi.cko
head: 2.73
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 73;    selected revisions: 3
description:
----------------------------
revision 2.26
date: 1995/06/14 16:35:58;  author: chip;  state: Exp;  lines: +0 -2
periodic checkin of Wed Jun 14 09:35:27 PDT 1995
----------------------------
revision 2.25
date: 1995/06/14 16:29:51;  author: chip;  state: Exp;  lines: +0 -1
periodic checkin of Wed Jun 14 09:29:49 PDT 1995
----------------------------
revision 2.24
date: 1995/06/14 16:24:08;  author: chip;  state: Exp;  lines: +3 -0
periodic checkin of Wed Jun 14 09:24:06 PDT 1995
=============================================================================

RCS file: /s6/cvsroot/euterpe/compass/layouts/vlsi.log,v
Working file: compass/layouts/vlsi.log
head: 2.88
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 88;    selected revisions: 3
description:
----------------------------
revision 2.28
date: 1995/06/14 16:35:59;  author: chip;  state: Exp;  lines: +3 -0
periodic checkin of Wed Jun 14 09:35:27 PDT 1995
----------------------------
revision 2.27
date: 1995/06/14 16:29:53;  author: chip;  state: Exp;  lines: +1 -0
periodic checkin of Wed Jun 14 09:29:49 PDT 1995
----------------------------
revision 2.26
date: 1995/06/14 16:24:09;  author: chip;  state: Exp;  lines: +3 -0
periodic checkin of Wed Jun 14 09:24:06 PDT 1995
=============================================================================

RCS file: /s6/cvsroot/euterpe/doc/BOM,v
Working file: doc/BOM
head: 22.5
branch:
locks: strict
access list:
```

```
keyword substitution: kv
total revisions: 70;    selected revisions: 1
description:
BOM for doc
----------------------------
revision 20.1
date: 1995/06/15 00:11:32;  author: bobm;  state: Exp;  lines: +11 -11
Release Target: euterpe/doc
      front.mif
      intro.mif
      opcodes.mif
      pipeline.mif
      memory.mif
      events.mif
      reset.mif
      clock.mif
      cerberus.mif
      endian.mif
      newchanges.mif

only a few small changes
=============================================================================

RCS file: /s6/cvsroot/euterpe/doc/Attic/cerberus.mif,v
Working file: doc/cerberus.mif
head: 4.39
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 53;    selected revisions: 1
description:
----------------------------
revision 4.36
date: 1995/06/15 00:08:07;  author: bobm;  state: Exp;  lines: +47 -169
periodic checkin. only a few small changes.
=============================================================================

RCS file: /s6/cvsroot/euterpe/doc/Attic/clock.mif,v
Working file: doc/clock.mif
head: 19.6
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 6;     selected revisions: 1
description:
----------------------------
revision 19.6
date: 1995/06/15 00:07:32;  author: bobm;  state: Exp;  lines: +54 -63
periodic checkin. only a few small changes.
=============================================================================

RCS file: /s6/cvsroot/euterpe/doc/Attic/endian.mif,v
Working file: doc/endian.mif
head: 19.6
branch:
```

```
locks: strict
access list:
keyword substitution: kv
total revisions: 6;     selected revisions: 1
description:
----------------------------
revision 19.6
date: 1995/06/15 00:08:30;  author: bobm;  state: Exp;  lines: +155 -163
periodic checkin. only a few small changes.
=============================================================================

RCS file: /s6/cvsroot/euterpe/doc/Attic/events.mif,v
Working file: doc/events.mif
head: 4.24
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 28;    selected revisions: 1
description:
----------------------------
revision 4.24
date: 1995/06/15 00:07:04;  author: bobm;  state: Exp;  lines: +19 -710
periodic checkin. only a few small changes.
=============================================================================

RCS file: /s6/cvsroot/euterpe/doc/Attic/intro.mif,v
Working file: doc/intro.mif
head: 4.22
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 26;    selected revisions: 1
description:
----------------------------
revision 4.22
date: 1995/06/15 00:04:48;  author: bobm;  state: Exp;  lines: +161 -422
periodic checkin. only a few small changes.
=============================================================================

RCS file: /s6/cvsroot/euterpe/doc/Attic/memory.mif,v
Working file: doc/memory.mif
head: 4.36
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 46;    selected revisions: 1
description:
----------------------------
revision 4.35
date: 1995/06/15 00:06:34;  author: bobm;  state: Exp;  lines: +79 -85
periodic checkin. only a few small changes.
=============================================================================

RCS file: /s6/cvsroot/euterpe/doc/Attic/newchanges.mif,v
```

```
Working file: doc/newchanges.mif
head: 16.13
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 13;    selected revisions: 1
description:
----------------------------
revision 16.12
date: 1995/06/15 00:08:37;  author: bobm;  state: Exp;  lines: +42 -23
periodic checkin. only a few small changes.
=============================================================================

RCS file: /s6/cvsroot/euterpe/doc/Attic/opcodes.mif,v
Working file: doc/opcodes.mif
head: 4.24
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 39;    selected revisions: 1
description:
----------------------------
revision 4.24
date: 1995/06/15 00:05:15;  author: bobm;  state: Exp;  lines: +35 -74
periodic checkin. only a few small changes.
=============================================================================

RCS file: /s6/cvsroot/euterpe/doc/Attic/pipeline.mif,v
Working file: doc/pipeline.mif
head: 4.24
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 27;    selected revisions: 1
description:
----------------------------
revision 4.24
date: 1995/06/15 00:05:51;  author: bobm;  state: Exp;  lines: +203 -1014
periodic checkin. only a few small changes.
=============================================================================

RCS file: /s6/cvsroot/euterpe/doc/Attic/reset.mif,v
Working file: doc/reset.mif
head: 4.22
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 26;    selected revisions: 1
description:
----------------------------
revision 4.22
date: 1995/06/15 00:07:20;  author: bobm;  state: Exp;  lines: +47 -317
periodic checkin. only a few small changes.
```

```
=============================================================================

RCS file: /s6/cvsroot/euterpe/verify/BOM,v
Working file: verify/BOM
head: 12.34
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 404;   selected revisions: 7
description:
----------------------------
revision 4.185
date: 1995/06/15 16:45:31;  author: jeffm;  state: Exp;  lines: +2 -2
Release Target: euterpe/verify/nasty

Oops, prior release contained downlevel files.
----------------------------
revision 4.184
date: 1995/06/15 16:42:36;  author: jeffm;  state: Exp;  lines: +2 -2
Release Target: euterpe/verify/nasty

Fixed hermnasty.
----------------------------
revision 4.183
date: 1995/06/13 19:56:29;  author: jeffm;  state: Exp;  lines: +2 -2
Release Target: euterpe/verify/toplevel
      uunb_debug.srl

For debugging uu/nb handshake
----------------------------
revision 4.182
date: 1995/06/13 18:27:09;  author: jeffm;  state: Exp;  lines: +2 -2
Release Target: euterpe/verify/toplevel
      hermnasty_debug.srl

Fix more signal names
----------------------------
revision 4.181
date: 1995/06/13 18:24:21;  author: jeffm;  state: Exp;  lines: +2 -2
Release Target: euterpe/verify/toplevel
      ife_debug.srl

For hermestestCOMO
----------------------------
revision 4.180
date: 1995/06/13 18:07:27;  author: jeffm;  state: Exp;  lines: +2 -2
Release Target: euterpe/verify/toplevel
      hermnasty_debug.srl

Fix signal names
----------------------------
revision 4.179
date: 1995/06/13 17:49:27;  author: jeffm;  state: Exp;  lines: +2 -2
Release Target: euterpe/verify/toplevel
      hermnasty_debug.srl
```

```
New trace file for Zycad
============================================================================

RCS file: /s6/cvsroot/euterpe/verify/nasty/BOM,v
Working file: verify/nasty/BOM
head: 19.0
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 36;    selected revisions: 4
description:
releasebom adding BOM
----------------------------
revision 18.0
date: 1995/06/15 16:45:16;  author: jeffm;  state: Exp;  lines: +1 -1
Release Target: euterpe/verify/nasty

Oops, prior release contained downlevel files.
----------------------------
revision 17.1
date: 1995/06/15 16:45:07;  author: jeffm;  state: Exp;  lines: +5 -5
releasebom: File needs to be up-to-date to use commit -r
----------------------------
revision 17.0
date: 1995/06/15 16:42:23;  author: jeffm;  state: Exp;  lines: +1 -1
Release Target: euterpe/verify/nasty

Fixed hermnasty.
----------------------------
revision 16.1
date: 1995/06/15 16:42:15;  author: jeffm;  state: Exp;  lines: +6 -6
releasebom: File needs to be up-to-date to use commit -r
============================================================================

RCS file: /s6/cvsroot/euterpe/verify/nasty/hermnasty.S,v
Working file: verify/nasty/hermnasty.S
head: 1.15
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 15;    selected revisions: 1
description:
----------------------------
revision 1.12
date: 1995/06/15 16:40:03;  author: jeffm;  state: Exp;  lines: +26 -21
Fixed test.

1) The LVA bit used to indicate uncached access was also used in hermes
module calculation. Fixed to use bit 39 instead.

2) Was checking wrong address when checking event register after causing
I/O rupts.

3) Was using wrong bits to force blocking reads to return. The cylinders weren't
enabled for some of the bits that were returned.
```

```
=============================================================================

RCS file: /s6/cvsroot/euterpe/verify/perf/eshufflei4mux_perf.S,v
Working file: verify/perf/eshufflei4mux_perf.S
head: 1.3
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 3;     selected revisions: 1
description:
----------------------------
revision 1.2
date: 1995/06/15 22:47:21;  author: claseman;  state: Exp;  lines: +13 -2
new scheme for cycle adjustment
=============================================================================

RCS file: /s6/cvsroot/euterpe/verify/perf/gcompress16_perf.S,v
Working file: verify/perf/gcompress16_perf.S
head: 3.3
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 3;     selected revisions: 1
description:
----------------------------
revision 3.2
date: 1995/06/15 22:47:26;  author: claseman;  state: Exp;  lines: +15 -1
new scheme for cycle adjustment
=============================================================================

RCS file: /s6/cvsroot/euterpe/verify/perf/gcompress64_perf.S,v
Working file: verify/perf/gcompress64_perf.S
head: 3.3
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 3;     selected revisions: 1
description:
----------------------------
revision 3.2
date: 1995/06/15 22:47:28;  author: claseman;  state: Exp;  lines: +15 -1
new scheme for cycle adjustment
=============================================================================

RCS file: /s6/cvsroot/euterpe/verify/perf/gextracti128_perf.S,v
Working file: verify/perf/gextracti128_perf.S
head: 1.3
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 3;     selected revisions: 1
description:
----------------------------
```

```
revision 1.2
date: 1995/06/15 22:47:24;  author: claseman;  state: Exp;  lines: +13 -2
new scheme for cycle adjustment
=============================================================================

RCS file: /s6/cvsroot/euterpe/verify/perf/gextracti64_perf.S,v
Working file: verify/perf/gextracti64_perf.S
head: 1.3
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 3;     selected revisions: 1
description:
----------------------------
revision 1.2
date: 1995/06/15 22:47:22;  author: claseman;  state: Exp;  lines: +13 -2
new scheme for cycle adjustment
=============================================================================

RCS file: /s6/cvsroot/euterpe/verify/perf/ggfmul8_perf.S,v
Working file: verify/perf/ggfmul8_perf.S
head: 1.3
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 3;     selected revisions: 1
description:
----------------------------
revision 1.2
date: 1995/06/15 23:04:45;  author: claseman;  state: Exp;  lines: +13 -2
new scheme for cycle adjustment
=============================================================================

RCS file: /s6/cvsroot/euterpe/verify/perf/gmuladd16_perf.S,v
Working file: verify/perf/gmuladd16_perf.S
head: 1.3
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 3;     selected revisions: 1
description:
----------------------------
revision 1.2
date: 1995/06/14 22:28:34;  author: claseman;  state: Exp;  lines: +13 -2
cycle correction adjustment
=============================================================================

RCS file: /s6/cvsroot/euterpe/verify/perf/gmuladd32_perf.S,v
Working file: verify/perf/gmuladd32_perf.S
head: 1.3
branch:
locks: strict
access list:
keyword substitution: kv
```

```
total revisions: 3;     selected revisions: 1
description:
----------------------------
revision 1.2
date: 1995/06/14 22:28:32;  author: claseman;  state: Exp;  lines: +13 -2
cycle correction adjustment
=============================================================================

RCS file: /s6/cvsroot/euterpe/verify/perf/gmuladd64_perf.S,v
Working file: verify/perf/gmuladd64_perf.S
head: 1.4
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 4;     selected revisions: 2
description:
----------------------------
revision 1.3
date: 1995/06/14 22:27:05;  author: claseman;  state: Exp;  lines: +3 -3
correction to cycle adjustment
----------------------------
revision 1.2
date: 1995/06/14 21:52:49;  author: claseman;  state: Exp;  lines: +13 -2
setup new scheme for cycle correction
=============================================================================

RCS file: /s6/cvsroot/euterpe/verify/perf/gmuladd8_perf.S,v
Working file: verify/perf/gmuladd8_perf.S
head: 1.3
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 3;     selected revisions: 1
description:
----------------------------
revision 1.2
date: 1995/06/14 22:28:36;  author: claseman;  state: Exp;  lines: +13 -2
cycle correction adjustment
=============================================================================

RCS file: /s6/cvsroot/euterpe/verify/perf/icachemiss_perf.S,v
Working file: verify/perf/icachemiss_perf.S
head: 1.10
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 10;    selected revisions: 1
description:
----------------------------
revision 1.2
date: 1995/06/12 16:12:31;  author: claseman;  state: Exp;  lines: +1 -1
use TAG_SPACING
=============================================================================
```

```
RCS file: /s6/cvsroot/euterpe/verify/random/Makefile,v
Working file: verify/random/Makefile
head: 1.20
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 20;    selected revisions: 1
description:
----------------------------
revision 1.20
date: 1995/06/15 19:38:53;  author: dit00;  state: Exp;  lines: +6 -1
Fix rebuild to build _1 files.
=============================================================================

RCS file: /s6/cvsroot/euterpe/verify/random/regdepend_r1001.S,v
Working file: verify/random/regdepend_r1001.S
head: 3.3
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 3;     selected revisions: 1
description:
----------------------------
revision 3.2
date: 1995/06/15 19:39:32;  author: dit00;  state: Exp;  lines: +8 -8
Change gcopyswapiswap instruction to gcopyswapi11
=============================================================================

RCS file: /s6/cvsroot/euterpe/verify/random/regdepend_r1122.S,v
Working file: verify/random/regdepend_r1122.S
head: 3.2
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 2;     selected revisions: 1
description:
----------------------------
revision 3.1
date: 1995/06/15 19:40:57;  author: dit00;  state: Exp;
New test, ran ok.
=============================================================================

RCS file: /s6/cvsroot/euterpe/verify/random/regdepend_r1578.S,v
Working file: verify/random/regdepend_r1578.S
head: 3.3
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 3;     selected revisions: 1
description:
----------------------------
revision 3.2
date: 1995/06/15 19:49:30;  author: dit00;  state: Exp;  lines: +11 -11
```

```
 Change gcopyswapiswap instruction to gcopyswapi11
=============================================================================

RCS file: /s6/cvsroot/euterpe/verify/random/regdepend_r1639.S,v
Working file: verify/random/regdepend_r1639.S
head: 3.2
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 2;     selected revisions: 1
description:
----------------------------
revision 3.1
date: 1995/06/15 19:49:49;  author: dit00;  state: Exp;
New test, ran ok
=============================================================================

RCS file: /s6/cvsroot/euterpe/verify/random/regdepend_r1742.S,v
Working file: verify/random/regdepend_r1742.S
head: 3.3
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 3;     selected revisions: 1
description:
----------------------------
revision 3.2
date: 1995/06/15 19:50:13;  author: dit00;  state: Exp;  lines: +10 -10
 Change gcopyswapiswap instruction to gcopyswapi11
=============================================================================

RCS file: /s6/cvsroot/euterpe/verify/random/regdepend_r1794.S,v
Working file: verify/random/regdepend_r1794.S
head: 2.3
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 3;     selected revisions: 1
description:
----------------------------
revision 2.2
date: 1995/06/15 19:50:31;  author: dit00;  state: Exp;  lines: +11 -11
 Change gcopyswapiswap instruction to gcopyswapi11
=============================================================================

RCS file: /s6/cvsroot/euterpe/verify/random/regdepend_r1847.S,v
Working file: verify/random/regdepend_r1847.S
head: 3.2
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 2;     selected revisions: 1
description:
```

```
----------------------------
revision 3.1
date: 1995/06/15 19:50:41;  author: dit00;  state: Exp;
New test, ran ok
=============================================================================

RCS file: /s6/cvsroot/euterpe/verify/random/regdepend_r1906.S,v
Working file: verify/random/regdepend_r1906.S
head: 3.3
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 3;     selected revisions: 1
description:
----------------------------
revision 3.2
date: 1995/06/15 19:50:59;  author: dit00;  state: Exp;  lines: +8 -8
 Change gcopyswapiswap instruction to gcopyswapi11
=============================================================================

RCS file: /s6/cvsroot/euterpe/verify/random/regdepend_r1937.S,v
Working file: verify/random/regdepend_r1937.S
head: 2.3
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 3;     selected revisions: 1
description:
----------------------------
revision 2.2
date: 1995/06/15 19:51:11;  author: dit00;  state: Exp;  lines: +14 -14
 Change gcopyswapiswap instruction to gcopyswapi11
=============================================================================

RCS file: /s6/cvsroot/euterpe/verify/random/regdepend_r2057.S,v
Working file: verify/random/regdepend_r2057.S
head: 3.2
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 2;     selected revisions: 1
description:
----------------------------
revision 3.1
date: 1995/06/15 19:51:23;  author: dit00;  state: Exp;
New test, ran ok
=============================================================================

RCS file: /s6/cvsroot/euterpe/verify/random/regdepend_r2079.S,v
Working file: verify/random/regdepend_r2079.S
head: 2.3
branch:
locks: strict
access list:
```

```
keyword substitution: kv
total revisions: 3;     selected revisions: 1
description:
----------------------------
revision 2.2
date: 1995/06/15 19:51:38;  author: dit00;  state: Exp;  lines: +7 -7
 Change gcopyswapiswap instruction to gcopyswapi11
=============================================================================

RCS file: /s6/cvsroot/euterpe/verify/random/regdepend_r2226.S,v
Working file: verify/random/regdepend_r2226.S
head: 2.3
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 3;     selected revisions: 1
description:
----------------------------
revision 2.2
date: 1995/06/15 19:51:55;  author: dit00;  state: Exp;  lines: +12 -12
 Change gcopyswapiswap instruction to gcopyswapi11
=============================================================================

RCS file: /s6/cvsroot/euterpe/verify/random/regdepend_r2368.S,v
Working file: verify/random/regdepend_r2368.S
head: 2.3
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 3;     selected revisions: 1
description:
----------------------------
revision 2.2
date: 1995/06/15 19:52:08;  author: dit00;  state: Exp;  lines: +12 -12
 Change gcopyswapiswap instruction to gcopyswapi11
=============================================================================

RCS file: /s6/cvsroot/euterpe/verify/random/regdepend_r393.S,v
Working file: verify/random/regdepend_r393.S
head: 2.2
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 2;     selected revisions: 1
description:
----------------------------
revision 2.2
date: 1995/06/15 19:52:17;  author: dit00;  state: Exp;  lines: +8 -8
 Change gcopyswapiswap instruction to gcopyswapi11
=============================================================================

RCS file: /s6/cvsroot/euterpe/verify/random/regdepend_r3957.S,v
Working file: verify/random/regdepend_r3957.S
head: 3.2
```

```
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 2;     selected revisions: 1
description:
----------------------------
revision 3.1
date: 1995/06/12 20:59:01;  author: dit00;  state: Exp;
Test ran ok
=============================================================================

RCS file: /s6/cvsroot/euterpe/verify/random/regdepend_r4157.S,v
Working file: verify/random/regdepend_r4157.S
head: 3.2
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 2;     selected revisions: 1
description:
----------------------------
revision 3.1
date: 1995/06/12 20:58:03;  author: dit00;  state: Exp;
Test ran ok
=============================================================================

RCS file: /s6/cvsroot/euterpe/verify/random/regdepend_r521.S,v
Working file: verify/random/regdepend_r521.S
head: 2.3
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 3;     selected revisions: 1
description:
----------------------------
revision 2.2
date: 1995/06/15 19:52:34;  author: dit00;  state: Exp;  lines: +12 -12
 Change gcopyswapiswap instruction to gcopyswapi11
=============================================================================

RCS file: /s6/cvsroot/euterpe/verify/random/regdepend_r5564.S,v
Working file: verify/random/regdepend_r5564.S
head: 2.3
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 3;     selected revisions: 1
description:
----------------------------
revision 2.2
date: 1995/06/15 19:52:44;  author: dit00;  state: Exp;  lines: +13 -13
 Change gcopyswapiswap instruction to gcopyswapi11
=============================================================================
```

```
RCS file: /s6/cvsroot/euterpe/verify/random/regdepend_r5712.S,v
Working file: verify/random/regdepend_r5712.S
head: 2.3
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 3;     selected revisions: 1
description:
----------------------------
revision 2.2
date: 1995/06/15 19:52:53;  author: dit00;  state: Exp;  lines: +10 -10
 Change gcopyswapiswap instruction to gcopyswapi11
=============================================================================

RCS file: /s6/cvsroot/euterpe/verify/random/regdepend_r5854.S,v
Working file: verify/random/regdepend_r5854.S
head: 2.3
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 3;     selected revisions: 1
description:
----------------------------
revision 2.2
date: 1995/06/15 19:53:00;  author: dit00;  state: Exp;  lines: +14 -14
 Change gcopyswapiswap instruction to gcopyswapi11
=============================================================================

RCS file: /s6/cvsroot/euterpe/verify/random/regdepend_r5996.S,v
Working file: verify/random/regdepend_r5996.S
head: 2.3
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 3;     selected revisions: 1
description:
----------------------------
revision 2.2
date: 1995/06/15 19:53:08;  author: dit00;  state: Exp;  lines: +10 -10
 Change gcopyswapiswap instruction to gcopyswapi11
=============================================================================

RCS file: /s6/cvsroot/euterpe/verify/random/regdepend_r6143.S,v
Working file: verify/random/regdepend_r6143.S
head: 2.3
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 3;     selected revisions: 1
description:
----------------------------
revision 2.2
date: 1995/06/15 19:53:18;  author: dit00;  state: Exp;  lines: +10 -10
```

```
 Change gcopyswapiswap instruction to gcopyswapi11
=============================================================================

RCS file: /s6/cvsroot/euterpe/verify/random/regdepend_r6308.S,v
Working file: verify/random/regdepend_r6308.S
head: 2.3
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 3;     selected revisions: 1
description:
----------------------------
revision 2.2
date: 1995/06/15 19:53:26;  author: dit00;  state: Exp;  lines: +10 -10
 Change gcopyswapiswap instruction to gcopyswapi11
=============================================================================

RCS file: /s6/cvsroot/euterpe/verify/random/regdepend_r6450.S,v
Working file: verify/random/regdepend_r6450.S
head: 2.3
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 3;     selected revisions: 1
description:
----------------------------
revision 2.2
date: 1995/06/15 19:53:33;  author: dit00;  state: Exp;  lines: +7 -7
 Change gcopyswapiswap instruction to gcopyswapi11
=============================================================================

RCS file: /s6/cvsroot/euterpe/verify/random/regdepend_r656.S,v
Working file: verify/random/regdepend_r656.S
head: 2.3
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 3;     selected revisions: 1
description:
----------------------------
revision 2.2
date: 1995/06/15 19:53:48;  author: dit00;  state: Exp;  lines: +6 -6
 Change gcopyswapiswap instruction to gcopyswapi11
=============================================================================

RCS file: /s6/cvsroot/euterpe/verify/random/regdepend_r6597.S,v
Working file: verify/random/regdepend_r6597.S
head: 2.3
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 3;     selected revisions: 1
description:
```

```
----------------------------
revision 2.2
date: 1995/06/15 19:54:00;  author: dit00;  state: Exp;  lines: +8 -8
 Change gcopyswapiswap instruction to gcopyswapi11
=============================================================================

RCS file: /s6/cvsroot/euterpe/verify/random/regdepend_r6739.S,v
Working file: verify/random/regdepend_r6739.S
head: 2.3
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 3;     selected revisions: 1
description:
----------------------------
revision 2.2
date: 1995/06/15 19:54:19;  author: dit00;  state: Exp;  lines: +9 -9
 Change gcopyswapiswap instruction to gcopyswapi11
=============================================================================

RCS file: /s6/cvsroot/euterpe/verify/random/regdepend_r6881.S,v
Working file: verify/random/regdepend_r6881.S
head: 2.3
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 3;     selected revisions: 1
description:
----------------------------
revision 2.2
date: 1995/06/15 19:54:25;  author: dit00;  state: Exp;  lines: +10 -10
 Change gcopyswapiswap instruction to gcopyswapi11
=============================================================================

RCS file: /s6/cvsroot/euterpe/verify/random/regdepend_r7210.S,v
Working file: verify/random/regdepend_r7210.S
head: 2.3
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 3;     selected revisions: 1
description:
----------------------------
revision 2.2
date: 1995/06/15 19:54:30;  author: dit00;  state: Exp;  lines: +4 -4
 Change gcopyswapiswap instruction to gcopyswapi11
=============================================================================

RCS file: /s6/cvsroot/euterpe/verify/random/regdepend_r7338.S,v
Working file: verify/random/regdepend_r7338.S
head: 2.3
branch:
locks: strict
access list:
```

```
keyword substitution: kv
total revisions: 3;     selected revisions: 1
description:
----------------------------
revision 2.2
date: 1995/06/15 19:54:38;  author: dit00;  state: Exp;  lines: +10 -10
 Change gcopyswapiswap instruction to gcopyswapi11
=============================================================================

RCS file: /s6/cvsroot/euterpe/verify/random/regdepend_r7495.S,v
Working file: verify/random/regdepend_r7495.S
head: 2.3
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 3;     selected revisions: 1
description:
----------------------------
revision 2.2
date: 1995/06/15 19:54:44;  author: dit00;  state: Exp;  lines: +9 -9
 Change gcopyswapiswap instruction to gcopyswapi11
=============================================================================

RCS file: /s6/cvsroot/euterpe/verify/random/regdepend_r754.S,v
Working file: verify/random/regdepend_r754.S
head: 3.2
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 2;     selected revisions: 1
description:
----------------------------
revision 3.1
date: 1995/06/15 16:18:48;  author: dit00;  state: Exp;
Test ran OK.
=============================================================================

RCS file: /s6/cvsroot/euterpe/verify/random/regdepend_r7623.S,v
Working file: verify/random/regdepend_r7623.S
head: 2.3
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 3;     selected revisions: 1
description:
----------------------------
revision 2.2
date: 1995/06/15 19:54:51;  author: dit00;  state: Exp;  lines: +12 -12
 Change gcopyswapiswap instruction to gcopyswapi11
=============================================================================

RCS file: /s6/cvsroot/euterpe/verify/random/regdepend_r7751.S,v
Working file: verify/random/regdepend_r7751.S
head: 2.3
```

```
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 3;     selected revisions: 1
description:
----------------------------
revision 2.2
date: 1995/06/15 19:54:58;  author: dit00;  state: Exp;  lines: +11 -11
 Change gcopyswapiswap instruction to gcopyswapi11
=============================================================================

RCS file: /s6/cvsroot/euterpe/verify/random/regdepend_r786.S,v
Working file: verify/random/regdepend_r786.S
head: 2.3
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 3;     selected revisions: 1
description:
----------------------------
revision 2.2
date: 1995/06/15 19:55:06;  author: dit00;  state: Exp;  lines: +4 -4
 Change gcopyswapiswap instruction to gcopyswapi11
=============================================================================

RCS file: /s6/cvsroot/euterpe/verify/random/regdepend_r915.S,v
Working file: verify/random/regdepend_r915.S
head: 2.3
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 3;     selected revisions: 1
description:
----------------------------
revision 2.2
date: 1995/06/15 19:55:14;  author: dit00;  state: Exp;  lines: +13 -13
 Change gcopyswapiswap instruction to gcopyswapi11
=============================================================================

RCS file: /s6/cvsroot/euterpe/verify/random/status,v
Working file: verify/random/status
head: 2.26
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 26;    selected revisions: 1
description:
----------------------------
revision 2.10
date: 1995/06/15 19:55:20;  author: dit00;  state: Exp;  lines: +16 -0
Update
=============================================================================
```

```
RCS file: /s6/cvsroot/euterpe/verify/random/template,v
Working file: verify/random/template
head: 2.33
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 33;    selected revisions: 1
description:
----------------------------
revision 2.9
date: 1995/06/15 19:55:40;  author: dit00;  state: Exp;  lines: +45 -40
Update
=============================================================================

RCS file: /s6/cvsroot/euterpe/verify/standalone/hc/Makefile,v
Working file: verify/standalone/hc/Makefile
head: 1.38
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 38;    selected revisions: 1
description:
----------------------------
revision 1.38
date: 1995/06/16 00:17:33;  author: brian;  state: Exp;  lines: +8 -2
Added DUMPFILE command line switch to re-direct verilog dumpfiles.
=============================================================================

RCS file: /s6/cvsroot/euterpe/verify/standalone/hc/NOTES,v
Working file: verify/standalone/hc/NOTES
head: 1.28
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 28;    selected revisions: 2
description:
----------------------------
revision 1.27
date: 1995/06/14 20:53:22;  author: brian;  state: Exp;  lines: +3 -0
Adde some notes about the 'termite' test.
----------------------------
revision 1.26
date: 1995/06/14 20:51:52;  author: brian;  state: Exp;  lines: +8 -1
Added termite (woody bug) into regression. Fixed onechan to have tag
field of 0 for octlet writes.
=============================================================================

RCS file: /s6/cvsroot/euterpe/verify/standalone/hc/nbhc_drive.V,v
Working file: verify/standalone/hc/nbhc_drive.V
head: 1.55
branch:
locks: strict
access list:
keyword substitution: kv
```

```
total revisions: 55;    selected revisions: 3
description:
----------------------------
revision 1.51
date: 1995/06/16 00:17:35;  author: brian;  state: Exp;  lines: +13 -3
Added DUMPFILE command line switch to re-direct verilog dumpfiles.
----------------------------
revision 1.50
date: 1995/06/14 20:33:24;  author: brian;  state: Exp;  lines: +2 -2
Changed default dumpfile directory back to current directory.
----------------------------
revision 1.49
date: 1995/06/13 21:45:05;  author: brian;  state: Exp;  lines: +2 -2
Fixed MGsend delay bug in driver. Driver was checked-in with wrong value.
=============================================================================

RCS file: /s6/cvsroot/euterpe/verify/standalone/hc/nbhcregress,v
Working file: verify/standalone/hc/nbhcregress
head: 5.14
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 14;    selected revisions: 1
description:
----------------------------
revision 5.13
date: 1995/06/14 20:51:54;  author: brian;  state: Exp;  lines: +1 -0
Added termite (woody bug) into regression. Fixed onechan to have tag
field of 0 for octlet writes.
=============================================================================

RCS file: /s6/cvsroot/euterpe/verify/standalone/hc/onechan.vec,v
Working file: verify/standalone/hc/onechan.vec
head: 2.3
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 3;     selected revisions: 1
description:
----------------------------
revision 2.3
date: 1995/06/14 20:51:56;  author: brian;  state: Exp;  lines: +87 -3
Added termite (woody bug) into regression. Fixed onechan to have tag
field of 0 for octlet writes.
=============================================================================

RCS file: /s6/cvsroot/euterpe/verify/standalone/hc/termite.vec,v
Working file: verify/standalone/hc/termite.vec
head: 10.1
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 1;     selected revisions: 1
description:
```

```
----------------------------
revision 10.1
date: 1995/06/14 19:58:05;  author: brian;  state: Exp;
Bug with event sequence.
=============================================================================

RCS file: /s6/cvsroot/euterpe/verify/toplevel/BOM,v
Working file: verify/toplevel/BOM
head: 44.1
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 132;   selected revisions: 5
description:
releasebom adding BOM
----------------------------
revision 39.41
date: 1995/06/13 19:56:16;  author: jeffm;  state: Exp;  lines: +5 -1
Release Target: euterpe/verify/toplevel
      uunb_debug.srl

For debugging uu/nb handshake
----------------------------
revision 39.40
date: 1995/06/13 18:26:52;  author: jeffm;  state: Exp;  lines: +2 -2
Release Target: euterpe/verify/toplevel
      hermnasty_debug.srl

Fix more signal names
----------------------------
revision 39.39
date: 1995/06/13 18:24:07;  author: jeffm;  state: Exp;  lines: +5 -1
Release Target: euterpe/verify/toplevel
      ife_debug.srl

For hermestestCOMO
----------------------------
revision 39.38
date: 1995/06/13 18:07:13;  author: jeffm;  state: Exp;  lines: +2 -2
Release Target: euterpe/verify/toplevel
      hermnasty_debug.srl

Fix signal names
----------------------------
revision 39.37
date: 1995/06/13 17:49:16;  author: jeffm;  state: Exp;  lines: +5 -1
Release Target: euterpe/verify/toplevel
      hermnasty_debug.srl

New trace file for Zycad
=============================================================================

RCS file: /s6/cvsroot/euterpe/verify/toplevel/hermnasty_debug.srl,v
Working file: verify/toplevel/hermnasty_debug.srl
head: 39.3
branch:
```

```
locks: strict
access list:
keyword substitution: kv
total revisions: 3;     selected revisions: 3
description:
----------------------------
revision 39.3
date: 1995/06/13 18:26:18;  author: jeffm;  state: Exp;  lines: +11 -2
Fix more signal names
----------------------------
revision 39.2
date: 1995/06/13 18:06:54;  author: jeffm;  state: Exp;  lines: +2 -2
Fix signal names.
----------------------------
revision 39.1
date: 1995/06/13 17:46:57;  author: jeffm;  state: Exp;
New trace file for Zycad
=============================================================================

RCS file: /s6/cvsroot/euterpe/verify/toplevel/ife_debug.srl,v
Working file: verify/toplevel/ife_debug.srl
head: 39.1
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 1;     selected revisions: 1
description:
----------------------------
revision 39.1
date: 1995/06/13 18:23:48;  author: jeffm;  state: Exp;
For hermestestCOMO
=============================================================================

RCS file: /s6/cvsroot/euterpe/verify/toplevel/uunb_debug.srl,v
Working file: verify/toplevel/uunb_debug.srl
head: 39.1
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 1;     selected revisions: 1
description:
----------------------------
revision 39.1
date: 1995/06/13 19:55:56;  author: jeffm;  state: Exp;
For debugging uu/nb handshake
=============================================================================

RCS file: /s6/cvsroot/euterpe/verilog/BOM,v
Working file: verilog/BOM
head: 6.9
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 1390;  selected revisions: 6
```

```
description:
top level verilog BOM
----------------------------
revision 3.627
date: 1995/06/14 22:35:47;  author: mws;  state: Exp;  lines: +2 -2
Release Target: euterpe/verilog/bsrc

uu/uu_control.pim:
  Update for 15jun95's uu/uu.V uu/uuthruut.Veqn uu/uustepuu.pla:
  Change in bsrc BOM 320.1-320.2/321.0 and bsrc/uu BOM 206-7.0 to try to
  suppress forward progress before new store&swap algorithms set its repel
  state still was not working.  It was needed on eta3 but the addition
  of a pipeline that could support eta3 was forgotten and eta0 pipe was
  improperly sustituted.  Change swpBsy pipe to flops to handle all etas.
  Then ustepuu loses 1 dontcare step, but uuthruut can dontcare eta3 enforcement
  on step 1 (restore 1.12).  Hopefully this will stop synch ops from losing CC
  in the middle of their algorithms, (cachesynchnasty_0 performance 50% worse).
cj/rupt.tst cj/rsrvd.tst:  Delay expected event mode exit from BBack
  to BBackBrk to match bsrc/BOM 319.0 and uu/BOM 204.0.
----------------------------
revision 3.626
date: 1995/06/14 08:39:37;  author: mws;  state: Exp;  lines: +2 -2
Release Target: euterpe/verilog/bsrc/uu

uu/uu.V uu/uuthruut.Veqn uu/uustepuu.pla uu/sswap(8).tst:
  Change in bsrc BOM 320.1-320.2/321.0 and bsrc/uu BOM 206-7.0 to try to
  suppress forward progress before new store&swap algorithms set its repel
  state still was not working.  It was needed on eta3 but the addition
  of a pipeline that could support eta3 was forgotten and eta0 pipe was
  improperly sustituted.  Change swpBsy pipe to flops to handle all etas.
  Then ustepuu loses 1 dontcare step, but uuthruut can dontcare eta3 enforcement
  on step 1 (restore 1.12).  Restore sswap(8).tst to match (125.4(169.2))
  only to avoid confusion of BOM not using newest files).
  Do placement tomorrow.  Hopefully this will stop synch ops from losing CC in
  the middle of their algorithms, (cachesynchnasty_0 performance 50% worse).
----------------------------
revision 3.625
date: 1995/06/12 04:52:07;  author: mws;  state: Exp;  lines: +2 -2
Release Target: euterpe/verilog/bsrc

uu/uu_control.pim for uu/uu.V uu/uuthruut.Veqn uu/uustepuu.pla(comments only)
----------------------------
revision 3.624
date: 1995/06/11 19:36:06;  author: mws;  state: Exp;  lines: +2 -2
Release Target: euterpe/verilog/bsrc/uu

uu/uu.V (do placement later):
  Change in bsrc BOM 320.1 and bsrc/uu BOM 206.0 to "use the swpBsy pipe to
  suppress forward progress early in the store&swap until the repel can take
  over" was allowing a store&swap (synch op) in one cyl to suppress forward
  progress in up to 3 other cyls.  The claim was that this would not matter
  architecturally, although it would perturb micro level behavior.  Further
  reflection has deemed this too tricky, so add eta chopper so that only the
  cyl needing suppression gets it.
uu/sswap.tst uu/uusswap8.tst:  Restore previous versions to match restore of
  1st job in store&swap again enforcing eta3.  Doing restore only to avoid
  confusion of the BOM including not-the-newest file from the repository.
```

```
----------------------------
revision 3.623
date: 1995/06/11 08:36:18;  author: mws;  state: Exp;  lines: +2 -2
Release Target: euterpe/verilog/bsrc/uu

uu/uu.V uu/uuthruut.Veqn uu/uustepuu.pla(comments only)  (do placement later):
  Change in bsrc BOM 319.0 and bsrc/uu BOM 204.0 to "set repel and enforce eta
  for the remaining volatile synch op (store&swap) sequence at the end of the
  2nd (was 1st) job" inadvertently allowed forward progress to be declared,
  releasing CC after an ICache miss before DCache miss was tested.  This
  allowed another cyl to steal the ICache line, undoing the previous fill
  and causing a thrash hang.  To avoid the expense of adding a forward
  progress pipe, we justify the use of the swpBsy pipe to suppress
  forward progress early in the store&swap until the repel can take over.
----------------------------
revision 3.622
date: 1995/06/10 09:08:03;  author: mws;  state: Exp;  lines: +2 -2
Release Target: euterpe/verilog/bsrc

StoreSwaps (atomic/synch ops) were mostly broken because:
uu/uu.V:
  Pipelining typo in yesterday's change used stepUV instead of UW in computing
  vldSwpGoUW, causing probable excess repel toggels leaving preempts locked
  out (hangs) or sequences unprotected (integrity damage).
uu/uustepuu.pla:
  Yesterday's change forgot to remove dontcares no longer available when
  storeswap repel begin delay was overloaded onto swpBsy.
uu/uuswap.tst uu/uuswap8.tst:  Update to match yesterday's change to wait until
  step=1 to align eta and begin repel.
=============================================================================

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/BOM,v
Working file: verilog/bsrc/BOM
head: 346.6
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 1737;  selected revisions: 9
description:
----------------------------
revision 322.0
date: 1995/06/14 22:35:29;  author: mws;  state: Exp;  lines: +1 -1
Release Target: euterpe/verilog/bsrc

uu/uu_control.pim:
  Update for 15jun95's uu/uu.V uu/uuthruut.Veqn uu/uustepuu.pla:
  Change in bsrc BOM 320.1-320.2/321.0 and bsrc/uu BOM 206-7.0 to try to
  suppress forward progress before new store&swap algorithms set its repel
  state still was not working.  It was needed on eta3 but the addition
  of a pipeline that could support eta3 was forgotten and eta0 pipe was
  improperly sustituted.  Change swpBsy pipe to flops to handle all etas.
  Then ustepuu loses 1 dontcare step, but uuthruut can dontcare eta3 enforcement
  on step 1 (restore 1.12).  Hopefully this will stop synch ops from losing CC
  in the middle of their algorithms, (cachesynchnasty_0 performance 50% worse).
cj/rupt.tst cj/rsrvd.tst:  Delay expected event mode exit from BBack
  to BBackBrk to match bsrc/BOM 319.0 and uu/BOM 204.0.
```

```
----------------------------
revision 321.2
date: 1995/06/14 22:35:17;  author: mws;  state: Exp;  lines: +3 -3
releasebom: File needs to be up-to-date to use commit -r
----------------------------
revision 321.1
date: 1995/06/14 08:39:22;  author: mws;  state: Exp;  lines: +2 -2
Release Target: euterpe/verilog/bsrc/uu

uu/uu.V uu/uuthruut.Veqn uu/uustepuu.pla uu/sswap(8).tst:
  Change in bsrc BOM 320.1-320.2/321.0 and bsrc/uu BOM 206-7.0 to try to
  suppress forward progress before new store&swap algorithms set its repel
  state still was not working.  It was needed on eta3 but the addition
  of a pipeline that could support eta3 was forgotten and eta0 pipe was
  improperly sustituted.  Change swpBsy pipe to flops to handle all etas.
  Then ustepuu loses 1 dontcare step, but uuthruut can dontcare eta3 enforcement
  on step 1 (restore 1.12).  Restore sswap(8).tst to match (125.4(169.2))
  only to avoid confusion of BOM not using newest files).
  Do placement tomorrow.  Hopefully this will stop synch ops from losing CC in
  the middle of their algorithms, (cachesynchnasty_0 performance 50% worse).
----------------------------
revision 321.0
date: 1995/06/12 04:51:47;  author: mws;  state: Exp;  lines: +1 -1
Release Target: euterpe/verilog/bsrc

uu/uu_control.pim for uu/uu.V uu/uuthruut.Veqn uu/uustepuu.pla(comments only)
----------------------------
revision 320.3
date: 1995/06/12 04:51:34;  author: mws;  state: Exp;  lines: +2 -2
releasebom: File needs to be up-to-date to use commit -r
----------------------------
revision 320.2
date: 1995/06/11 19:35:45;  author: mws;  state: Exp;  lines: +2 -2
Release Target: euterpe/verilog/bsrc/uu

uu/uu.V (do placement later):
  Change in bsrc BOM 320.1 and bsrc/uu BOM 206.0 to "use the swpBsy pipe to
  suppress forward progress early in the store&swap until the repel can take
  over" was allowing a store&swap (synch op) in one cyl to suppress forward
  progress in up to 3 other cyls.  The claim was that this would not matter
  architecturally, although it would perturb micro level behavior.  Further
  reflection has deemed this too tricky, so add eta chopper so that only the
  cyl needing suppression gets it.
uu/sswap.tst uu/uusswap8.tst:  Restore previous versions to match restore of
  1st job in store&swap again enforcing eta3.  Doing restore only to avoid
  confusion of the BOM including not-the-newest file from the repository.
----------------------------
revision 320.1
date: 1995/06/11 08:36:03;  author: mws;  state: Exp;  lines: +2 -2
Release Target: euterpe/verilog/bsrc/uu

uu/uu.V uu/uuthruut.Veqn uu/uustepuu.pla(comments only)  (do placement later):
  Change in bsrc BOM 319.0 and bsrc/uu BOM 204.0 to "set repel and enforce eta
  for the remaining volatile synch op (store&swap) sequence at the end of the
  2nd (was 1st) job" inadvertently allowed forward progress to be declared,
  releasing CC after an ICache miss before DCache miss was tested.  This
  allowed another cyl to steal the ICache line, undoing the previous fill
```

```
  and causing a thrash hang.  To avoid the expense of adding a forward
  progress pipe, we justify the use of the swpBsy pipe to suppress
  forward progress early in the store&swap until the repel can take over.
----------------------------
revision 320.0
date: 1995/06/10 09:07:40;  author: mws;  state: Exp;  lines: +1 -1
Release Target: euterpe/verilog/bsrc

StoreSwaps (atomic/synch ops) were mostly broken because:
uu/uu.V:
  Pipelining typo in yesterday's change used stepUV instead of UW in computing
  vldSwpGoUW, causing probable excess repel toggels leaving preempts locked
  out (hangs) or sequences unprotected (integrity damage).
uu/uustepuu.pla:
  Yesterday's change forgot to remove dontcares no longer available when
  storeswap repel begin delay was overloaded onto swpBsy.
uu/uuswap.tst uu/uuswap8.tst:  Update to match yesterday's change to wait until
  step=1 to align eta and begin repel.
----------------------------
revision 319.2
date: 1995/06/10 09:07:23;  author: mws;  state: Exp;  lines: +2 -2
releasebom: File needs to be up-to-date to use commit -r
=============================================================================

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/Makefile.tst,v
Working file: verilog/bsrc/Makefile.tst
head: 40.104
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 104;   selected revisions: 2
description:
----------------------------
revision 40.84
date: 1995/06/13 06:58:18;  author: tbr;  state: Exp;  lines: +6 -5
use nof data for incomplete nets in final report
----------------------------
revision 40.83
date: 1995/06/11 01:09:17;  author: tbr;  state: Exp;  lines: +22 -9
name .slack file consistently.  New hueristig for all net file ordering
=============================================================================

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/chip_euterpe-base.netcap,v
Working file: verilog/bsrc/chip_euterpe-base.netcap
head: 312.20
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 20;    selected revisions: 1
description:
----------------------------
revision 312.2
date: 1995/06/10 18:52:01;  author: tbr;  state: Exp;  lines: +76524 -88341
from latest BOM 318 run
=============================================================================
```

```
RCS file: /s6/cvsroot/euterpe/verilog/bsrc/chip_euterpe-base.nof,v
Working file: verilog/bsrc/chip_euterpe-base.nof
head: 307.11
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 11;    selected revisions: 1
description:
----------------------------
revision 307.5
date: 1995/06/10 19:04:24;  author: tbr;  state: Exp;  lines: +15247 -15247
from latest BOM 318 run
=============================================================================

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/chip_euterpe-base.pim,v
Working file: verilog/bsrc/chip_euterpe-base.pim
head: 312.23
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 23;    selected revisions: 1
description:
----------------------------
revision 312.2
date: 1995/06/10 18:55:55;  author: tbr;  state: Exp;  lines: +53247 -53731
from latest BOM 318 run
=============================================================================

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/chip_euterpe-base.strength,v
Working file: verilog/bsrc/chip_euterpe-base.strength
head: 312.20
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 20;    selected revisions: 1
description:
----------------------------
revision 312.2
date: 1995/06/10 18:57:06;  author: tbr;  state: Exp;  lines: +49897 -58001
from latest BOM 318 run
=============================================================================

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/chip_euterpe-base.xrf,v
Working file: verilog/bsrc/chip_euterpe-base.xrf
head: 307.11
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 11;    selected revisions: 1
description:
----------------------------
revision 307.5
```

```
date: 1995/06/10 19:06:51;  author: tbr;  state: Exp;  lines: +25167 -25169
from latest BOM 318 run
=============================================================================

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/pimlib.pl,v
Working file: verilog/bsrc/pimlib.pl
head: 37.8
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 8;     selected revisions: 1
description:
----------------------------
revision 37.7
date: 1995/06/11 01:05:49;  author: tbr;  state: Exp;  lines: +6 -1
handle .flipx correctly
=============================================================================

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/cj/BOM,v
Working file: verilog/bsrc/cj/BOM
head: 122.0
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 259;   selected revisions: 2
description:
----------------------------
revision 120.0
date: 1995/06/14 22:30:06;  author: mws;  state: Exp;  lines: +1 -1
Release Target: euterpe/verilog/bsrc

uu/uu_control.pim:
  Update for 15jun95's uu/uu.V uu/uuthruut.Veqn uu/uustepuu.pla:
  Change in bsrc BOM 320.1-320.2/321.0 and bsrc/uu BOM 206-7.0 to try to
  suppress forward progress before new store&swap algorithms set its repel
  state still was not working.  It was needed on eta3 but the addition
  of a pipeline that could support eta3 was forgotten and eta0 pipe was
  improperly sustituted.  Change swpBsy pipe to flops to handle all etas.
  Then ustepuu loses 1 dontcare step, but uuthruut can dontcare eta3 enforcement
  on step 1 (restore 1.12).  Hopefully this will stop synch ops from losing CC
  in the middle of their algorithms, (cachesynchnasty_0 performance 50% worse).
cj/rupt.tst cj/rsrvd.tst:  Delay expected event mode exit from BBack
  to BBackBrk to match bsrc/BOM 319.0 and uu/BOM 204.0.
----------------------------
revision 119.1
date: 1995/06/14 22:29:59;  author: mws;  state: Exp;  lines: +3 -3
releasebom: File needs to be up-to-date to use commit -r
=============================================================================

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/cj/rsrvd.tst,v
Working file: verilog/bsrc/cj/rsrvd.tst
head: 78.13
branch:
locks: strict
access list:
```

```
keyword substitution: kv
total revisions: 13;    selected revisions: 1
description:
----------------------------
revision 78.12
date: 1995/06/14 22:27:12;  author: mws;  state: Exp;  lines: +2 -2
cj/rupt.tst cj/rsrvd.tst:  Delay expected event mode exit from BBack
  to BBackBrk to match bsrc/BOM 319.0 and uu/BOM 204.0.
=============================================================================

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/cj/rupt.tst,v
Working file: verilog/bsrc/cj/rupt.tst
head: 93.5
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 5;     selected revisions: 1
description:
----------------------------
revision 93.4
date: 1995/06/14 22:27:14;  author: mws;  state: Exp;  lines: +2 -2
cj/rupt.tst cj/rsrvd.tst:  Delay expected event mode exit from BBack
  to BBackBrk to match bsrc/BOM 319.0 and uu/BOM 204.0.
=============================================================================

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/hc/hc.V,v
Working file: verilog/bsrc/hc/hc.V
head: 1.56
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 56;    selected revisions: 1
description:
----------------------------
revision 1.53
date: 1995/06/15 16:30:46;  author: woody;  state: Exp;  lines: +15 -6
hc.V, hc_ostate.pla:
When a conflict on a load is detected, it is possible to recive another request
for nb. This resulted in hc keeping track of two requests. If the second
requests was an Event Daemon Store, it could be processed out of order (before
the conflicting load is resolved and sent to the hermes interface). This
resulted in an incorrect tag being sent to nb creating confusion. Also
hc_brrresp is assuming that ostate will be processing the Blocking Read
immediately, which isn't the case following a conflicting load. This resulted
in the channel hanging. Hermesnasty discovered this problem. The logic has been
changed so that the 'br' controls are held pending until the conflict is
resolved and the load is transmitted.
Furthermore by inspection it was discovered that ostate was not correctly
updating address/controls (frcSadrSnap) following the tranmit of a conflicting
load. The result being that conflictRecovery mode stayed active too long with a
minor impact to performance.

placement updates to follow.
=============================================================================
```

```
RCS file: /s6/cvsroot/euterpe/verilog/bsrc/hc/hc_ostate.pla,v
Working file: verilog/bsrc/hc/hc_ostate.pla
head: 3.26
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 26;    selected revisions: 1
description:
----------------------------
revision 3.24
date: 1995/06/15 16:30:48;  author: woody;  state: Exp;  lines: +10 -4
hc.V, hc_ostate.pla:
When a conflict on a load is detected, it is possible to recive another request
for nb. This resulted in hc keeping track of two requests. If the second
requests was an Event Daemon Store, it could be processed out of order (before
the conflicting load is resolved and sent to the hermes interface). This
resulted in an incorrect tag being sent to nb creating confusion. Also
hc_brrresp is assuming that ostate will be processing the Blocking Read
immediately, which isn't the case following a conflicting load. This resulted
in the channel hanging. Hermesnasty discovered this problem. The logic has been
changed so that the 'br' controls are held pending until the conflict is
resolved and the load is transmitted.
Furthermore by inspection it was discovered that ostate was not correctly
updating address/controls (frcSadrSnap) following the tranmit of a conflicting
load. The result being that conflictRecovery mode stayed active too long with a
minor impact to performance.

placement updates to follow.
=============================================================================

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/uu/BOM,v
Working file: verilog/bsrc/uu/BOM
head: 218.1
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 480;   selected revisions: 12
description:
----------------------------
revision 210.0
date: 1995/06/14 22:34:17;  author: mws;  state: Exp;  lines: +1 -1
Release Target: euterpe/verilog/bsrc

uu/uu_control.pim:
  Update for 15jun95's uu/uu.V uu/uuthruut.Veqn uu/uustepuu.pla:
  Change in bsrc BOM 320.1-320.2/321.0 and bsrc/uu BOM 206-7.0 to try to
  suppress forward progress before new store&swap algorithms set its repel
  state still was not working.  It was needed on eta3 but the addition
  of a pipeline that could support eta3 was forgotten and eta0 pipe was
  improperly sustituted.  Change swpBsy pipe to flops to handle all etas.
  Then ustepuu loses 1 dontcare step, but uuthruut can dontcare eta3 enforcement
  on step 1 (restore 1.12).  Hopefully this will stop synch ops from losing CC
  in the middle of their algorithms, (cachesynchnasty_0 performance 50% worse).
cj/rupt.tst cj/rsrvd.tst:  Delay expected event mode exit from BBack
  to BBackBrk to match bsrc/BOM 319.0 and uu/BOM 204.0.
```

```
----------------------------
revision 209.1
date: 1995/06/14 22:34:09;  author: mws;  state: Exp;  lines: +2 -2
releasebom: File needs to be up-to-date to use commit -r
----------------------------
revision 209.0
date: 1995/06/14 08:39:04;  author: mws;  state: Exp;  lines: +1 -1
Release Target: euterpe/verilog/bsrc/uu

uu/uu.V uu/uuthruut.Veqn uu/uustepuu.pla uu/sswap(8).tst:
  Change in bsrc BOM 320.1-320.2/321.0 and bsrc/uu BOM 206-7.0 to try to
  suppress forward progress before new store&swap algorithms set its repel
  state still was not working.  It was needed on eta3 but the addition
  of a pipeline that could support eta3 was forgotten and eta0 pipe was
  improperly sustituted.  Change swpBsy pipe to flops to handle all etas.
  Then ustepuu loses 1 dontcare step, but uuthruut can dontcare eta3 enforcement
  on step 1 (restore 1.12).  Restore sswap(8).tst to match (125.4(169.2))
  only to avoid confusion of BOM not using newest files).
  Do placement tomorrow.  Hopefully this will stop synch ops from losing CC in
  the middle of their algorithms, (cachesynchnasty_0 performance 50% worse).
----------------------------
revision 208.1
date: 1995/06/14 08:38:54;  author: mws;  state: Exp;  lines: +6 -6
releasebom: File needs to be up-to-date to use commit -r
----------------------------
revision 208.0
date: 1995/06/12 04:50:25;  author: mws;  state: Exp;  lines: +1 -1
Release Target: euterpe/verilog/bsrc

uu/uu_control.pim for uu/uu.V uu/uuthruut.Veqn uu/uustepuu.pla(comments only)
----------------------------
revision 207.1
date: 1995/06/12 04:50:17;  author: mws;  state: Exp;  lines: +2 -2
releasebom: File needs to be up-to-date to use commit -r
----------------------------
revision 207.0
date: 1995/06/11 19:35:23;  author: mws;  state: Exp;  lines: +1 -1
Release Target: euterpe/verilog/bsrc/uu

uu/uu.V (do placement later):
  Change in bsrc BOM 320.1 and bsrc/uu BOM 206.0 to "use the swpBsy pipe to
  suppress forward progress early in the store&swap until the repel can take
  over" was allowing a store&swap (synch op) in one cyl to suppress forward
  progress in up to 3 other cyls.  The claim was that this would not matter
  architecturally, although it would perturb micro level behavior.  Further
  reflection has deemed this too tricky, so add eta chopper so that only the
  cyl needing suppression gets it.
uu/sswap.tst uu/uusswap8.tst:  Restore previous versions to match restore of
  1st job in store&swap again enforcing eta3.  Doing restore only to avoid
  confusion of the BOM including not-the-newest file from the repository.
----------------------------
revision 206.1
date: 1995/06/11 19:35:13;  author: mws;  state: Exp;  lines: +4 -4
releasebom: File needs to be up-to-date to use commit -r
----------------------------
revision 206.0
date: 1995/06/11 08:35:45;  author: mws;  state: Exp;  lines: +1 -1
```

```
Release Target: euterpe/verilog/bsrc/uu

uu/uu.V uu/uuthruut.Veqn uu/uustepuu.pla(comments only)  (do placement later):
  Change in bsrc BOM 319.0 and bsrc/uu BOM 204.0 to "set repel and enforce eta
  for the remaining volatile synch op (store&swap) sequence at the end of the
  2nd (was 1st) job" inadvertently allowed forward progress to be declared,
  releasing CC after an ICache miss before DCache miss was tested.  This
  allowed another cyl to steal the ICache line, undoing the previous fill
  and causing a thrash hang.  To avoid the expense of adding a forward
  progress pipe, we justify the use of the swpBsy pipe to suppress
  forward progress early in the store&swap until the repel can take over.
----------------------------
revision 205.1
date: 1995/06/11 08:35:36;  author: mws;  state: Exp;  lines: +4 -4
releasebom: File needs to be up-to-date to use commit -r
----------------------------
revision 205.0
date: 1995/06/10 09:06:13;  author: mws;  state: Exp;  lines: +1 -1
Release Target: euterpe/verilog/bsrc

StoreSwaps (atomic/synch ops) were mostly broken because:
uu/uu.V:
  Pipelining typo in yesterday's change used stepUV instead of UW in computing
  vldSwpGoUW, causing probable excess repel toggels leaving preempts locked
  out (hangs) or sequences unprotected (integrity damage).
uu/uustepuu.pla:
  Yesterday's change forgot to remove dontcares no longer available when
  storeswap repel begin delay was overloaded onto swpBsy.
uu/uuswap.tst uu/uuswap8.tst:  Update to match yesterday's change to wait until
  step=1 to align eta and begin repel.
----------------------------
revision 204.1
date: 1995/06/10 09:06:03;  author: mws;  state: Exp;  lines: +5 -5
releasebom: File needs to be up-to-date to use commit -r
=============================================================================

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/uu/sswap.tst,v
Working file: verilog/bsrc/uu/sswap.tst
head: 125.8
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 8;     selected revisions: 3
description:
----------------------------
revision 125.6
date: 1995/06/14 08:36:09;  author: mws;  state: Exp;  lines: +5 -5
uu/uu.V uu/uuthruut.Veqn uu/uustepuu.pla uu/sswap(8).tst:
  Change in bsrc BOM 320.1-320.2/321.0 and bsrc/uu BOM 206-7.0 to try to
  suppress forward progress before new store&swap algorithms set its repel
  state still was not working.  It was needed on eta3 but the addition
  of a pipeline that could support eta3 was forgotten and eta0 pipe was
  improperly sustituted.  Change swpBsy pipe to flops to handle all etas.
  Then ustepuu loses 1 dontcare step, but uuthruut can dontcare eta3 enforcement
  on step 1 (restore 1.12).  Restore sswap(8).tst to match (125.4(169.2))
  only to avoid confusion of BOM not using newest files).
```

```
  Do placement tomorrow.  Hopefully this will stop synch ops from losing CC in
  the middle of their algorithms, (cachesynchnasty_0 performance 50% worse).
----------------------------
revision 125.5
date: 1995/06/11 19:33:29;  author: mws;  state: Exp;  lines: +4 -4
uu/sswap.tst uu/uusswap8.tst:  Restore previous versions to match restore of
  1st job in store&swap again enforcing eta3.  Doing restore only to avoid
  confusion of the BOM including not-the-newest file from the repository.
----------------------------
revision 125.4
date: 1995/06/10 08:56:53;  author: mws;  state: Exp;  lines: +5 -5
StoreSwaps (atomic/synch ops) were mostly broken because:
uu/uu.V:
  Pipelining typo in yesterday's change used stepUV instead of UW in computing
  vldSwpGoUW, causing probable excess repel toggels leaving preempts locked
  out (hangs) or sequences unprotected (integrity damage).
uu/uustepuu.pla:
  Yesterday's change forgot to remove dontcares no longer available when
  storeswap repel begin delay was overloaded onto swpBsy.
uu/uuswap.tst uu/uuswap8.tst:  Update to match yesterday's change to wait until
  step=1 to align eta and begin repel.
=============================================================================

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/uu/sswap8.tst,v
Working file: verilog/bsrc/uu/sswap8.tst
head: 169.4
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 4;     selected revisions: 3
description:
----------------------------
revision 169.4
date: 1995/06/14 08:36:10;  author: mws;  state: Exp;  lines: +9 -9
uu/uu.V uu/uuthruut.Veqn uu/uustepuu.pla uu/sswap(8).tst:
  Change in bsrc BOM 320.1-320.2/321.0 and bsrc/uu BOM 206-7.0 to try to
  suppress forward progress before new store&swap algorithms set its repel
  state still was not working.  It was needed on eta3 but the addition
  of a pipeline that could support eta3 was forgotten and eta0 pipe was
  improperly sustituted.  Change swpBsy pipe to flops to handle all etas.
  Then ustepuu loses 1 dontcare step, but uuthruut can dontcare eta3 enforcement
  on step 1 (restore 1.12).  Restore sswap(8).tst to match (125.4(169.2))
  only to avoid confusion of BOM not using newest files).
  Do placement tomorrow.  Hopefully this will stop synch ops from losing CC in
  the middle of their algorithms, (cachesynchnasty_0 performance 50% worse).
----------------------------
revision 169.3
date: 1995/06/11 19:33:32;  author: mws;  state: Exp;  lines: +8 -8
uu/sswap.tst uu/uusswap8.tst:  Restore previous versions to match restore of
  1st job in store&swap again enforcing eta3.  Doing restore only to avoid
  confusion of the BOM including not-the-newest file from the repository.
----------------------------
revision 169.2
date: 1995/06/10 08:56:56;  author: mws;  state: Exp;  lines: +9 -9
StoreSwaps (atomic/synch ops) were mostly broken because:
uu/uu.V:
```

```
  Pipelining typo in yesterday's change used stepUV instead of UW in computing
  vldSwpGoUW, causing probable excess repel toggels leaving preempts locked
  out (hangs) or sequences unprotected (integrity damage).
uu/uustepuu.pla:
  Yesterday's change forgot to remove dontcares no longer available when
  storeswap repel begin delay was overloaded onto swpBsy.
uu/uuswap.tst uu/uuswap8.tst:  Update to match yesterday's change to wait until
  step=1 to align eta and begin repel.
=============================================================================

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/uu/uu.V,v
Working file: verilog/bsrc/uu/uu.V
head: 1.202
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 202;   selected revisions: 4
description:
issue unit
----------------------------
revision 1.196
date: 1995/06/14 08:36:13;  author: mws;  state: Exp;  lines: +33 -29
uu/uu.V uu/uuthruut.Veqn uu/uustepuu.pla uu/sswap(8).tst:
  Change in bsrc BOM 320.1-320.2/321.0 and bsrc/uu BOM 206-7.0 to try to
  suppress forward progress before new store&swap algorithms set its repel
  state still was not working.  It was needed on eta3 but the addition
  of a pipeline that could support eta3 was forgotten and eta0 pipe was
  improperly sustituted.  Change swpBsy pipe to flops to handle all etas.
  Then ustepuu loses 1 dontcare step, but uuthruut can dontcare eta3 enforcement
  on step 1 (restore 1.12).  Restore sswap(8).tst to match (125.4(169.2))
  only to avoid confusion of BOM not using newest files).
  Do placement tomorrow.  Hopefully this will stop synch ops from losing CC in
  the middle of their algorithms, (cachesynchnasty_0 performance 50% worse).
----------------------------
revision 1.195
date: 1995/06/11 19:18:04;  author: mws;  state: Exp;  lines: +11 -4
Change in bsrc BOM 320.1 and bsrc/uu BOM 206.0 to "use the swpBsy pipe to
suppress forward progress early in the store&swap until the repel can take
over" was allowing a store&swap (synch op) in one cyl to suppress forward
progress in up to 3 other cyls.  The claim was that this would not matter
architecturally, although it would perturb micro level behavior.  Further
reflection has deemed this too tricky, so add eta chopper so that only the
cyl needing suppression gets it.
----------------------------
revision 1.194
date: 1995/06/11 08:34:50;  author: mws;  state: Exp;  lines: +4 -2
uu/uu.V uu/uuthruut.Veqn uu/uustepuu.pla(comments only):
  Change in bsrc BOM 319.0 and bsrc/uu BOM 204.0 to "set repel and enforce eta
  for the remaining volatile synch op (store&swap) sequence at the end of the
  2nd (was 1st) job" inadvertently allowed forward progress to be declared,
  releasing CC after an ICache miss before DCache miss was tested.  This
  allowed another cyl to steal the ICache line, undoing the previous fill
  and causing a thrash hang.  To avoid the expense of adding a forward
  progress pipe, we justify the use of the swpBsy pipe to suppress
  forward progress early in the store&swap until the repel can take over.
----------------------------
```

```
revision 1.193
date: 1995/06/10 08:57:02;  author: mws;  state: Exp;  lines: +2 -2
StoreSwaps (atomic/synch ops) were mostly broken because:
uu/uu.V:
  Pipelining typo in yesterday's change used stepUV instead of UW in computing
  vldSwpGoUW, causing probable excess repel toggels leaving preempts locked
  out (hangs) or sequences unprotected (integrity damage).
uu/uustepuu.pla:
  Yesterday's change forgot to remove dontcares no longer available when
  storeswap repel begin delay was overloaded onto swpBsy.
uu/uuswap.tst uu/uuswap8.tst:  Update to match yesterday's change to wait until
  step=1 to align eta and begin repel.
=============================================================================

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/uu/uu_control.pim,v
Working file: verilog/bsrc/uu/uu_control.pim
head: 68.60
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 60;    selected revisions: 2
description:
----------------------------
revision 68.59
date: 1995/06/14 22:27:59;  author: mws;  state: Exp;  lines: +68 -47
Update for 15jun95's uu/uu.V uu/uuthruut.Veqn uu/uustepuu.pla:
Change in bsrc BOM 320.1-320.2/321.0 and bsrc/uu BOM 206-7.0 to try to
suppress forward progress before new store&swap algorithms set its repel
state still was not working.  It was needed on eta3 but the addition
of a pipeline that could support eta3 was forgotten and eta0 pipe was
improperly sustituted.  Change swpBsy pipe to flops to handle all etas.
Then ustepuu loses 1 dontcare step, but uuthruut can dontcare eta3 enforcement
on step 1 (restore 1.12).  Hopefully this will stop synch ops from losing CC
in the middle of their algorithms, (cachesynchnasty_0 performance 50% worse).
----------------------------
revision 68.58
date: 1995/06/12 04:43:34;  author: mws;  state: Exp;  lines: +2 -0
uu/uu_control.pim uu/uu.V uu/uuthruut.Veqn uu/uustepuu.pla(comments only):
  Change in bsrc BOM 319.0 and bsrc/uu BOM 204.0 to "set repel and enforce eta
  for the remaining volatile synch op (store&swap) sequence at the end of the
  2nd (was 1st) job" inadvertently allowed forward progress to be declared,
  releasing CC after an ICache miss before DCache miss was tested.  This
  allowed another cyl to steal the ICache line, undoing the previous fill
  and causing a thrash hang.  To avoid the expense of adding a forward
  progress pipe, we justify the use of the swpBsy pipe to suppress
  forward progress early in the store&swap until the repel can take over.
=============================================================================

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/uu/uustepuu.pla,v
Working file: verilog/bsrc/uu/uustepuu.pla
head: 84.16
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 16;    selected revisions: 3
```

```
description:
----------------------------
revision 84.15
date: 1995/06/14 08:36:17;  author: mws;  state: Exp;  lines: +11 -9
uu/uu.V uu/uuthruut.Veqn uu/uustepuu.pla uu/sswap(8).tst:
  Change in bsrc BOM 320.1-320.2/321.0 and bsrc/uu BOM 206-7.0 to try to
  suppress forward progress before new store&swap algorithms set its repel
  state still was not working.  It was needed on eta3 but the addition
  of a pipeline that could support eta3 was forgotten and eta0 pipe was
  improperly sustituted.  Change swpBsy pipe to flops to handle all etas.
  Then ustepuu loses 1 dontcare step, but uuthruut can dontcare eta3 enforcement
  on step 1 (restore 1.12).  Restore sswap(8).tst to match (125.4(169.2))
  only to avoid confusion of BOM not using newest files).
  Do placement tomorrow.  Hopefully this will stop synch ops from losing CC in
  the middle of their algorithms, (cachesynchnasty_0 performance 50% worse).
----------------------------
revision 84.14
date: 1995/06/11 08:34:55;  author: mws;  state: Exp;  lines: +10 -8
uu/uu.V uu/uuthruut.Veqn uu/uustepuu.pla(comments only):
  Change in bsrc BOM 319.0 and bsrc/uu BOM 204.0 to "set repel and enforce eta
  for the remaining volatile synch op (store&swap) sequence at the end of the
  2nd (was 1st) job" inadvertently allowed forward progress to be declared,
  releasing CC after an ICache miss before DCache miss was tested.  This
  allowed another cyl to steal the ICache line, undoing the previous fill
  and causing a thrash hang.  To avoid the expense of adding a forward
  progress pipe, we justify the use of the swpBsy pipe to suppress
  forward progress early in the store&swap until the repel can take over.
----------------------------
revision 84.13
date: 1995/06/10 08:57:07;  author: mws;  state: Exp;  lines: +9 -8
StoreSwaps (atomic/synch ops) were mostly broken because:
uu/uu.V:
  Pipelining typo in yesterday's change used stepUV instead of UW in computing
  vldSwpGoUW, causing probable excess repel toggels leaving preempts locked
  out (hangs) or sequences unprotected (integrity damage).
uu/uustepuu.pla:
  Yesterday's change forgot to remove dontcares no longer available when
  storeswap repel begin delay was overloaded onto swpBsy.
uu/uuswap.tst uu/uuswap8.tst:  Update to match yesterday's change to wait until
  step=1 to align eta and begin repel.
=============================================================================

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/uu/uuthruut.Veqn,v
Working file: verilog/bsrc/uu/uuthruut.Veqn
head: 1.14
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 14;    selected revisions: 2
description:
Check each resource against its throughput limit; combine.
----------------------------
revision 1.14
date: 1995/06/14 08:36:19;  author: mws;  state: Exp;  lines: +5 -12
uu/uu.V uu/uuthruut.Veqn uu/uustepuu.pla uu/sswap(8).tst:
  Change in bsrc BOM 320.1-320.2/321.0 and bsrc/uu BOM 206-7.0 to try to
```

```
  suppress forward progress before new store&swap algorithms set its repel
  state still was not working.  It was needed on eta3 but the addition
  of a pipeline that could support eta3 was forgotten and eta0 pipe was
  improperly sustituted.  Change swpBsy pipe to flops to handle all etas.
  Then ustepuu loses 1 dontcare step, but uuthruut can dontcare eta3 enforcement
  on step 1 (restore 1.12).  Restore sswap(8).tst to match (125.4(169.2))
  only to avoid confusion of BOM not using newest files).
  Do placement tomorrow.  Hopefully this will stop synch ops from losing CC in
  the middle of their algorithms, (cachesynchnasty_0 performance 50% worse).
----------------------------
revision 1.13
date: 1995/06/11 08:34:57;  author: mws;  state: Exp;  lines: +12 -5
uu/uu.V uu/uuthruut.Veqn uu/uustepuu.pla(comments only):
  Change in bsrc BOM 319.0 and bsrc/uu BOM 204.0 to "set repel and enforce eta
  for the remaining volatile synch op (store&swap) sequence at the end of the
  2nd (was 1st) job" inadvertently allowed forward progress to be declared,
  releasing CC after an ICache miss before DCache miss was tested.  This
  allowed another cyl to steal the ICache line, undoing the previous fill
  and causing a thrash hang.  To avoid the expense of adding a forward
  progress pipe, we justify the use of the swpBsy pipe to suppress
  forward progress early in the store&swap until the repel can take over.
=============================================================================
```